Delay Analysis of a Current Source CMOS Inverter for use in Voltage Controlled Delay Lines

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I. INTRODUCTION

Voltage controlled delay elements play an important role in interpolating time functions inside clock cycles. An example is the delay chain based Delay Locked Loops (DLLs) where the delay elements are continuously adjusted to a time reference. Current starved (current shrinking) inverters are the most usual delay elements used in voltage controlled delay chains [1-4]. This simple configuration has a very non-linear delay characteristic, even if improved current mirror circuits are used [5]. Applications based on delay elements where the gain is dependent on the point of lock, like DLLs, seems to have more constant dynamic behavior if more linear delay elements are used. The delay element designed around an inverter loaded with a current source and an additional static inverter, performing buffering and signal reshaping, shows smaller differential non-linearity values, and thus it is more suitable for these applications.

Since analytical expressions are more useful in understanding the behavior of circuits because they give insight into the dependence on physical parameters, a simple analytical expression for the delay of an inverter with a current source is derived in Section II. In Section III results are extended to find the overall delay of the proposed element. In section IV an example shows the validation of results by a comparison with SPICE results. Section V is dedicated to conclusions.
B. Capacitor Charging Current

The capacitor charging current is determined by the control voltage \( V_C \), sizing of transistors M1 and M2 and current gain \( A_d \) of the current mirrors M2-M4 and M3-M5. The current \( I_{20} \) on transistors M1 and M2 could be calculated by means of (1), considering the appropriate transistor operating regions (assuming that \( V_C<V_{DSS}/2 \)), i.e., transistors M1 and M2 are conducting. M2 is diode connected and thus always in saturation, so two regions can be defined, corresponding to the PMOS transistor being in the linear and in the saturation regions. From the linear condition for a PMOS transistor \( V_{DS} \), \( V_{DS} \), and \( V_{GD} \), and taking into account that \( V_{GS} = V_{DD} + I_{DD} \), the PMOS transistor is in the linear region (region 1) if:

\[
I_{20} > \frac{K_{n}}{2} (V_C + V_T - V_N) ^2
\]  
and in the saturation region (region 2) if:

\[
I_{20} > \frac{K_{n}}{2} (V_C + V_T - V_N) ^2 \]  

The current \( I_{20} \) as a function of \( V_C \) in the two regions can now be calculated (assuming that \( V_{DD} = V_{DD} = V_{DD} \)).

Region 1 (linear): In this region the PMOS transistor is in the linear region and current \( I_{20} \) is given by:

\[
I_{20} = K_{n} \left[ (V_{DD} - V_T) W_{DSS} - 0.5V_{DD} ^2 \right] \]  

Substituting the corresponding values for \( V_{DSS} \) and \( V_{DD} \) and solving for \( I_{20} \), we obtain:

\[
I_{20} = \frac{K_{n}}{2} (V_C + V_T - V_N) ^2
\]

Figure 2 shows the normalized current as a function of \( V_C \), according to (3) and (5), for different values of \( K_{n} \). We can see that for values of \( K_{n} / K_{p} \geq 5 \) and for values of \( V_C \) in the range 0-2V a normalized current is approximately a linear function of \( V_C \). The current can thus be written as:

\[
I_{20} = I_{020}(1 - mV_C)
\]

where \( I_{020} \) is obtained from (5) for \( V_C = 0 \) and equals:

\[
I_{020} = \frac{K_{n}K_{p}}{2(K_{n} + K_{p})} (V_{DD} - V_T)^2
\]

To calculate \( m \) needs another point on the curve. To minimize the error for all values of \( K_{n} / K_{p} \), we consider the second point to be at the intersection of the \( I_{20} \) curve with the curve that delimits the two regions of the PMOS transistor as indicated by (2). Solving for equal values of \( I_{20} \), we obtain the corresponding point \((V_{DSS}, I_{20})\):

\[
V_{DSS} = \frac{V_{DD} - V_T}{1 + \frac{K_{n}}{K_{p}}}
\]

and:

where \( K_{p} \) is the gain of transistor M6. This equation can be simplified using the series expansion of the square-root, giving:

\[
I_{20} = \frac{I_{020}}{K_{n}K_{p}(K_{n} + K_{p})} \left( 1 - mV_C \right)
\]

C. The Delay Equation

To calculate the delay of the current source inverter one must calculate the initial capacitor voltage \( V_{C0} \) first. It is important to do this, as the delay is calculated in the falling edge, the gate of M6 is assumed to be at \( V_{DD} \) (input signal at high level) and the capacitor voltage constant and equal to its minimum value. In this condition the current in M6 equals the current in M5 with M6 in linear region. Equating the corresponding values of current we find that the initial capacitor voltage (equal to the \( V_{O} \) of M6) is given by:

\[
V_{C0} = \frac{1}{1 + \frac{A_{o}K_{n}K_{p}}{K_{n}K_{p}(K_{n} + K_{p})}} (1 - mV_C)
\]

provided that the subtracting term under the square-root is much smaller than one. This is a good approximation as we can see in Fig. 4. The errors in initial capacitor voltage are larger for small values of \( V_C \), or in other words for large values of charging current, and are not significant to the final delay value. Equation (14) could be simplified by means of (8), giving:

\[
V_{C0} = \frac{I_{0}}{K_{n}K_{p}(K_{n} + K_{p})} \left( 1 - mV_C \right)
\]

where \( I_{0} \) is the maximum capacitor charging current.

Figure 5 shows simulated output waveforms for various control voltages (from \( V_C = 0V \) to \( V_C = 2V \) with 0.5V step).
B. Capacitor Charging Current

The capacitor charging current is determined by the control voltage $V_c$, sizing of transistors M1 and M2 and current gain $A_t$ of the current mirrors M2-M4 and M3-M5. The current $I_o$ on transistors M1 and M2 could be calculated by means of (1), considering the appropriate transistor operating regions (assuming that $V_c < V_{dd} - V_{th}$, i.e., transistors M1 and M2 are conducting). M2 is diode connected and thus always in saturation, so two regions can be defined, corresponding to the PMOS transistor being in the linear and in the saturation regions. From the linear condition for a PMOS transistor $V_{GS} = V_{dd} - V_{th}$, and taking into account that $V_{GS} = V_{dd} - V_{th}$, the PMOS transistor is in the linear region (region 1) if:

$$I_o > \frac{K_N}{2} \left( V_c + V_{th} - V_N \right)^2$$  \hspace{1cm} (2)

and in the saturation region (region 2) if:

$$I_o > \frac{K_N}{2} \left( V_c + V_{th} - V_N \right)^2$$  \hspace{1cm} (3)

The current $I_o$ as a function of $V_c$ in the two regions can now be calculated (assuming that $V_{th} = V_{th} = V_{dd}/2$).

Region 1 (linear): In this region the PMOS transistor is in the linear region and current $I_o$ is given by:

$$I_o = \frac{Kn}{2(K_n + Kn)} \left(V_c - V_{th} - 0.5V_{dd} \right)^2$$  \hspace{1cm} (4)

Substituting the corresponding values for $V_{dd}$ and $V_{th}$ and solving for $I_o$, we obtain:

$$I_o = \frac{Kn}{2(K_n + Kn)} \left(V_c - \frac{V_{th}}{2} - 0.5V_{dd} \right)^2$$  \hspace{1cm} (5)

Region 2 (saturation): In this region the PMOS transistor is also saturated and the current is simply:

$$I_o = \frac{Kn}{2(K_n + Kn)} \left(V_c - V_{th} - V_N \right)^2$$  \hspace{1cm} (6)

Figure 2 shows the normalized current as a function of $V_c$, according to (5) and (6), for different values of $K_n/K_n$. We can see that for values of $K_n / K_n > 5$ and for values of $V_c$ in the range 0-2V a normalized current is approximately a linear function of $V_c$. The current can thus be written as:

$$I_o = I_o (1 - mV_c)$$  \hspace{1cm} (7)

where $I_o$ is obtained from (5) for $V_c = 0$ and equals:

$$I_o = \frac{Kn}{2(K_n + Kn)} \left(V_c - V_{th} \right)^2$$  \hspace{1cm} (8)

To calculate $m$ one needs another point on the curve. To minimize the error for all values of $K_n/K_n$, we consider the second point to be at the intersection of the $I_o$ curve with the curve that delimits the two regions of the PMOS transistor as indicated by (2). Solving for equal values of $I_o$, we obtain the corresponding point $(V_{GS}, I_o)_{GS}$.

$$V_{GS} = \frac{V_c - V_{th}}{K_n} \left[ 1 + \frac{K_n}{K_n} \right]$$  \hspace{1cm} (9)

and:

$$m = \frac{K_n}{K_n + Kn}$$  \hspace{1cm} (10)

Substituting (9) and (10) in (7), we obtain:

$$m = \frac{1 + \frac{K_n}{K_n}}{1 + \frac{K_n}{K_n}}$$  \hspace{1cm} (11)

Figure 3 shows normalized real, saturated and linear curves of current for $K_n/K_n = 5$.

The capacitor charging current (the current through M5) is modeled simply as the multiplying of the current $I_o$ by the current gain of the current mirrors $(A_t)$:

$$I_c = A_tI_o (1 - mV_c)$$  \hspace{1cm} (12)

C. Delay Equation

To calculate the delay of the current source inverter one must calculate the initial capacitor voltage ($V_{cap}$) first. In order to do this, as the delay is calculated in the falling edge, the gate of M6 is assumed to be at $V_{dd}$ (input signal at high level) and the capacitor voltage constant and equal to its initial value. In this condition the current in M6 equals the current in M5 with M6 in linear region. Equating the corresponding values of current we find that the initial capacitor voltage (equal to the $V_{dd}$ of M6) is given by:

$$V_{cap} = \left( V_{dd} - V_{th} \right) \left[ 1 + \frac{A_t K_n}{K_n (K_n + Kn)} \right] (1 - mV_c)$$  \hspace{1cm} (13)

provided that the subtracting term under the square-root is much smaller than one. This is a good approximation as we can see in Fig. 4. The errors in initial capacitor voltage are larger for small values of $V_{dd}$, or in other words for large values of charging current, and are not significant to the final delay value. Equation (14) could be simplified by means of (8), giving:

$$V_{cap} = \frac{I_o}{K_n (V_{dd} - V_{th})} (1 - mV_c)$$  \hspace{1cm} (15)

where $I_o = A_tI_o$ is the maximum capacitor charging current.

Figure 5 shows simulated output waveforms for various control voltages (from $V_c = 0V$ to $V_c = 2V$ with 0.5V step).
for a fall edge of the input pulse. The linear variation of capacitor voltage is in accordance with the assumed constant capacitor charging current, starting from a initial voltage linearly dependent on the control voltage. Finally, in order to find the delay dependence on physical parameters, we derive the analytical expression for the time needed for the capacitor voltage to reach \( V_{gs} + 2 \) (assuming that the input signal has a fall time much smaller than the delay time and delay measured at \( V_{gs} + 2 \)). The time needed for a charging current \( I_c \), given by (12), to produce a capacitor voltage change of \( \Delta V_{cap} (=V_{gs}+2- V_{cap}) \) is:

\[
I_c = C \frac{V_{gs} + 2}{2e(t_0 - mV_c)} K_e \frac{1}{K_e(V_{gs} + V_c)}
\]

which is the equation that models the delay of the current source inverter.

### III. OVERALL DELAY

To find the overall delay of the entire non-inverting delay cell, we must add the previously calculated delay \( t_{cap} \) to the delay of the static inverter \( t_{cap} \). The first delay model for the CMOS static inverter which includes the effect of the input waveform was presented by Holdi and Jeppson [8]. They show that for fast input ramps the propagation delay could be written as the sum of an initial delay (proportional to the input rise time) and a final delay (equal to the step delay). Similar results were obtained by Venem and Thordorsson [9]. The model was generalized by Kaye et al. [10] for exponential input waveforms and Sahauri and Newton [7] introduced the hyper-law MOSFET model to calculate the delay for short-channel transistors. Recently, results were extended by Jeppson [6] and Dutta et al. [11] to include any value of the rise time of the input ramps.

In this work we use the results of Dutta et al. [11] to find the delay of the static inverter over the whole range of input transition-times and fanouts \( f_o \). The expression that describes the delay is (cf. Eq. 11 in [11]):

\[
t_{SL} = 1 + \frac{a}{b} I_n D_{cap}
\]

where \( t_{SL}, a, b, I_n, \) and \( D_{cap} \) is the slope of the de asymptotic approximation of the curve for infinite input rise-times. If \( D_{cap} \) and \( a \) are properly determined, the delay could be accurately found, for a given \( f_o \), if the rise time \( t_{cap} \) of the input signal were given. Defining \( I_n \) as the time to capacitor charge from 0 to \( V_{gs} \), by the current \( I_c \) given by (12), we can write:

\[
I_n = \frac{V_{gs} + 2}{A_{Dcap}(1 - mV_c)}
\]

The overall delay is simply the sum of the individual delays given by (16) and (17).

\[
t_d = t_{cap} + t_{SL}
\]

### IV. RESULTS

In this section we will illustrate the validity of the proposed formulas in the design of non-inverting delay elements for use in voltage controlled delay chains. The results are compared with SPICE simulations using 1.2um CMOS technology. Some factors must be taken into account before use the derived formulas. Firstly, the capacitor must be large enough relatively to parasitic capacitors in order to minimize the errors due to variations on the latter. The value used in the calculations is 250fF. Secondly, for this technology the square law, long channel transistor model is only approximate, and results do not agree well with simulation (even if non-minimum transistor sizes are used). As a consequence the current gain \( A_i \) is smaller than the predicted value and the maximum current \( I_{cap} \) is not accurate. To overcome this problem we find the approximate transistor dimensions and capacitor value for a given overall delay \( t_d \) (note that the specifications for \( t_d \) can be derived from \( t_{cap} \) because \( t_{cap} \) can be approximated by results on [11]). Next, a simulation is performed with \( V_{gs} = 0V \) and the current in M1 and M5 is determined (to give a more accurate value for \( A_i \)). We also need to measure the initial capacitor voltage from \( V_{gs} = 0V \) and \( V_{gs} = 1V \) (this is a process similar to the method used by Dutta [11] for finding parameters \( a, b \) and \( D_{cap} \)). With these one-time simulation real parameters can be found for plotting accurate delay characteristics for the initial transistor sizing (see Appendix for derivation of the parameter evaluation). If the overall delay results are not satisfactory simple modifications on transistor dimensions are required. The inspection of the dependence of the final circuit on physical parameters gives a final result in a single iteration. Table I shows the final parameters obtained for a given circuit (note that the \( K_e \)'s are normalized with respect to \( K_e \), designed for a 1ns delay per cell.

The values of the parameters \( a, b \) and \( D_{cap} \) for the static inverter are determined by curve-fitting as suggested by Dutta [11] and in Fig. 6 they are shown to be in good agreement with SPICE simulations. The values of \( I_{cap} \) used for SPICE simulation are obtained from (18), for \( V_{cap} \) in the range 0-2V.

With the parameters shown in Table I (assuming that \( V_{cap} = V_{gs} = 0.75V \)), delays \( t_{cap}, t_{cap} \), and \( t_d \) obtained from (16), (17) and (19) are plotted in Fig. 7. The corresponding results obtained from SPICE are also plotted and show very good agreement with the theoretical formulation. The differential non-linearity between \( V_{cap} = 0V \) and \( V_{cap} = 2V \) is better than:

\[
\frac{dx}{dt} = \frac{V_{cap}}{2} \left( \frac{V_{gs} - V_{cap}}{2} \right) = 17
\]

This represents a differential non-linearity four times smaller than the obtained with pulse-shrinking buffer for the same variation of delay per cell (cf. [11]).

### V. CONCLUSION

Even with the required recalculations of the parameters for more accurate results, the proposed non-inverting delay element shows a quasi-linear voltage controlled delay characteristic which is more suitable for use as interpolating elements in voltage control delay chains as in DLL applications (the gain of DLL is less dependent on point of lock). The analytical expressions are simple and comprehensive and the dependence of the delay on physical parameters allowing, typically with only one iteration, the calculation of transistor dimensions for a given delay per cell of the delay chain.

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**APPENDIX**

For more accurate results it is convenient to find more accurate values \( K_e, K_e, \) and \( A_i \) (we assume that \( K_e = 1 \)). From the equation that describes the charging of a capacitor by a current \( I_c \), we can write for \( V_{cap} = 0V \):

\[
A_i = \frac{V_{gs} + 2 - V_{cap}}{t_{cap}} C \ln \frac{t_{cap}}{t_{cap} - t_{cap}}
\]

where \( V_{cap} \) is the initial capacitor voltage for \( V_{cap} = 0V \) is the corresponding simulated delay measured at \( V_{cap} = 2V \) and \( t_{cap} \) is the current through M1 for \( V_{cap} = 0V \). To find \( K_e \), we obtain from (13) (for \( V_{cap} = 0V \) and \( V_{cap} = 1V \)):

\[
m = \begin{cases} \frac{1 - \left( \frac{V_{cap}}{V_{cap}} \right)^2}{2 - n(V_{cap} - V_{cap})} & V_{cap} < V_{cap} \\ \frac{1 - \left( \frac{V_{cap}}{V_{cap}} \right)^2}{2 - n(V_{cap} - V_{cap})} & V_{cap} = V_{cap} \end{cases}
\]

where \( V_{cap} \) is the initial capacitor voltage for \( V_{cap} = 1V \). With the \( m \) value we can calculate \( K_e \) from (11) assuming that \( K_e = 1 \):

\[
K_e = \frac{n(V_{cap} - V_{cap})}{2 - n(V_{cap} - V_{cap})}
\]

Finally, from (13) with \( V_{cap} = 0V \), \( K_e \) can be calculated as:

\[
K_e = A_i C \ln \left( \frac{1}{1 - V_{cap}} \right)
\]
for a fall edge of the input pulse. The linear variation of the capacitor voltage is in accordance with the assumed constant capacitor charging current, starting from a initial voltage linearly dependent on the control voltage.

Finally, in order to find the delay dependence on physical parameters, we derive the analytical expression for the time needed for the capacitor voltage to reach $V_{in}/2$ (assuming that the input signal has a fall time much smaller than the delay time and delay measured at $V_{in}/2$). The time needed for a charging current $I_c$ given by (12), to produce a capacitor voltage change of $dV_{COP} (=V_{in}/2-V_{COP})$ is:

$$I_c = \frac{V_{in}}{2(\tau_c - m \tau_c)} \frac{1}{K_c(V_{in} - V_C)}$$

(16)

which is the equation that models the delay of the current source inverter.

III. OVERALL DELAY

To find the overall delay of the entire non-inverting delay cell, we must add the previously calculated delay ($\tau_{in}$) to the delay of the static inverter ($\tau_{sc}$).

The first delay model for the CMOS static inverter which includes the effect of the input waveform was presented by Hedinstierna and Jeppson [8]. They show that for fast input ramps the propagation delay could be written as the sum of an initial delay (proportional to the input rise time) and a final delay (equal to the step delay). Similar results were obtained by Venmuri and Thorbjørnsen [9]. The model was generalized by Kayssi et al. [10] for exponential input waveforms and Sakurai and Newton [7] introduced the $\alpha$-power-law MOSFET model to calculate the delay for short-channel transistors. Recently, results were extended by Jeppson [6] and Dutta et al. [11] to include any value of the rise time of the input ramps.

In this work we use the results of Dutta et al. [11] to find the delay of the static inverter over the whole range of input transition-times and fanouts ($\nu_c$). The expression that describes the delay is (cf. Eq. 11 in [11]):

$$\tau_{sc} = \frac{1 + 4 \alpha}{\rho} \frac{\rho}{\nu_c} D_{sc}(\tau_{sc})$$

(17)

where $\tau_{sc}, \rho$, and $D_{sc}(\tau_{sc})$ is the slope of the de asymptotic approximation of the curves for infinite input rise-times. If $D_{sc}(\tau_{sc})$ and $\rho$ are properly determined, the delay could be accurately found, for a given $\nu_c$, if the rise time ($\nu_c$) of the input signal were given. Defining $\nu_c$ as the time to capacitor charge from 0 to $V_{in}$, by the current $I_c$ given by (12), we can write:

$$\nu_c = \frac{V_{in}}{A_{sc0}(1-mV_C)}$$

(18)

The overall delay is simply the sum of the individual delays given by (16) and (17).

$$\tau = \tau_{in} + \tau_{sc}$$

(19)

IV. RESULTS

In this section we illustrate the validity of the proposed formulas in the design of non-inverting delay elements for use in voltage controlled delay chains. The results are compared with SPICE simulations using the 1.2um CMOS technology. Some factors must be taken into account before use the derived formulas. Firstly, the capacitor must be large enough relatively to parasitic capacitors in order to minimize the errors due to variations on the latter. The value used in the calculations is 250fF. Secondly, for this technology the square law, long channel transistor model is only approximate, and results do not agree well with simulation (even if non-minimum transistor sizes are used). As a consequence the current gain ($A_C$) is smaller than the predicted value and the maximum current $I_{O}$ is not accurate. To overcome this problem we find the approximate transistor dimensions and capacitor value for a given overall delay ($\tau_{sc}$) (note that the specifications for $\tau_{sc}$ can be derived from $\tau_c$ because $\tau_c$ can be approximated by results of [11]). Next, a simulation is performed with $V_{in}=0$V and the current in M1 and M5 is determined (to give a more accurate value for $A_C$). We also need to measure the initial capacitor voltage from $V_{in}=0$V and $V_{in}=1$V (this is a process similar to the method used by Dutta [11] for finding parameters $\alpha$, $\rho$ and $D_{sc}(\tau_{sc})$. With these one-time simulation real parameters can be found for plotting accurate delay characteristics for the initial transistor sizing (see Appendix for derivation of the parameter evaluation). If the overall delay results are not satisfactory, simple modifications on transistor dimensions are required. The inspection of the dependence of the final circuit on physical parameters gives a final result in a single iteration. Table I shows the final parameters obtained for a given circuit (note that the $K_{sc}$'s are normalized with respect to $K_{sc}$, designed for a 1ns delay per cell.

The values of the parameters $\alpha$, $\beta$ and $D_{sc}(\tau_{sc})$ for the static inverter are determined by curve-fitting as suggested by Dutta [11] and in Fig. 6 they are shown to be in good agreement with SPICE simulations. The values of $\nu_c$ used for SPICE simulation are obtained from (18), for $V_{in}$ in the range 0-2V.

With the parameters shown in Table I (assuming that $V_{COP}=0.75V$, delays $\tau_{in}$, $\tau_{sc}$ and $\tau_c$ obtained from (16), (17) and (19) are plotted in Fig. 7. The corresponding results obtained from SPICE are also plotted and show very good agreement with the theoretical formulation. The differential non-linearity between $V_{in}=0$V and $V_{in}=2$V is better than:

$$\frac{dv_{in}}{dv_{COP}} = \frac{\nu_c - \nu_{0v}}{2} = 17$$

(20)

This represents a differential non-linearity four times smaller than the obtained with pulse-shrinking buffer for the same variation of delay per cell (cf. [1]).

V. CONCLUSION

Even with the required recalculation of the parameters for more accurate results, the proposed non-inverting delay element shows a quasi-linear voltage controlled delay characteristic which is more suitable for use as interpolating elements in voltage control delay chains as in DLL applications (the gain of DLL is less dependent on point of lock). The analytical expressions are simple and comprehensive and show the dependence of the delay on physical parameters allowing, typically with only one iteration, the calculation of transistor dimensions for a given delay per cell of the delay chain.

APPENDIX

For more accurate results it is convenient to find more accurate values $K_{sc}$, $K_{sc}$ and $A_C$ (we assume that $K_{sc}=1$). From the equation that describes the charge of a capacitor by a current $I_C$, we can write for $V_{in}=0$V:

$$A_C = \frac{\nu_c(1 - \frac{V_{in}}{2})C}{\nu_c}$$

where $V_{COP}$ is the initial capacitor voltage for $V_{in}=0$V, $I_C$ is the corresponding simulated delay measured at $V_{in}/2$ and $I_{sc}$ is the current through M1 for $V_{in}=0$V. To find $K_{sc}$, we obtain from (13) (for $V_{in}=0$V and $V_{in}=1$V):

$$m = = \left(\frac{1 - \frac{V_{in}}{V_{COP}}}{1 - \frac{V_{in}}{V_{COP}}}\right) = \left(\frac{1 - \frac{V_{in}}{V_{COP}}}{1 - \frac{V_{in}}{V_{COP}}}\right)$$

where $V_{COP}$ is the initial capacitor voltage for $V_{in}=1$V. With the $m$ value we can calculate $K_{sc}$ from (11) assuming that $K_{sc}=1$:

$$K_{sc} = m\left(\frac{V_{in}-0V}{2}\right)$$

Finally, from (13) with $V_{in}=0$V, $K_{sc}$ can be calculated as:

$$K_{sc} = \frac{\nu_c}{A_C \nu_c}\left(1 - \frac{V_{in}}{V_{COP}}\right)$$
Modelo de Propagação de Banda Larga para a Faixa das Ondas Millimétricas

José Fernandes, José Neves

Resumo - Este artigo apresenta um novo modelo de propagação de banda larga para a faixa das ondas millimétricas, baseado na teoria da óptica geométrica. O modelo consiste num conjunto de equações derivadas da teoria da propagação e é usado em conta as características do ambiente de propagação bem como a localização das antenas de transmissão e receptores.

Os resultados obtidos com o modelo desenvolvido são muito próximos dos obtidos com um software de traçado de raios numa gama bastante variada de ambientes, e a comparação com medições experimentais demonstram a validade do modelo proposto.

Abstract - A new wide-band propagation channel model for the millimetre-wave band, based on high frequency ray theory approximation, is presented in this paper. This model consists of a set of simple equations derived from the propagation theory and is able to take into account the propagation environment characteristics as well as the location of the transceiver antennas and their radiation patterns.

The results obtained with the developed model agree quite well with the results obtained with a ray tracing tool in a relatively wide range of environments. Also a comparison with some measurements have shown the validity of the proposed model.

I. INTRODUÇÃO

O MBS (Mobile Broadband System), actualmente em estudo e desenvolvimento na Europa, destina-se a proporcionar aos utilizadores móveis um acesso rápido de base ATM (Asynchronous Transfer Mode) à futura rede de banda larga (B-ISDN: Broadband Integrated Services Digital Network)[1].

A especificação de uma interface rádio para o MBS representa um desafio considerável. A gama de serviços oferecidos será muito alargada, com uma grande variedade de características e requisitos, incluindo ritmos de transmissão superiores a 100 Mbps, muito acima dos ritmos usados nos sistemas de rádio móvel actualmente existentes. Por isso, será necessário recorrer às ondas milimétricas para as ligações rádio, uma vez que os elevados ritmos de transmissão do sistema exigem uma banda consideravelmente larga, para a qual não existe disponibilidade no espectro radioeléctrico abaixo dos 30 GHz. Assim foram provisoriamente alocadas as bandas 62-65 GHz e 65-66 GHz bem como 39.5-40.5 GHz e 42.5-43.5 GHz.

Como o desemprego de sistemas de elevada dívida é fortemente limitado pelo canal de propagação[2], é necessário usar modelos que tenham em conta as características de propagação de um ambiente específico bem como as antenas da estação móvel (EM) e da estação base (EB).

Este artigo apresenta um modelo analítico para ambientes interiores, e facilmente extensível a ambientes exteriores. O modelo permite obter a resposta impulsiva (RI) num dado ambiente tendo em conta a sua geometria, propriedades reflectoras, posições da EM e da EB e diagrama de radiação das antenas. Uma vez obtida a RI, é inmediato o cálculo dos parâmetros da dispersão temporal do canal e da potência recebida normalizada (PRN) para qualquer posição da EM. Este modelo será de bastante utilidade, tanto para fins de investigação ao nível de outros blocos do sistema de comunicação radio móvel, como para facilitar a tarefa do engenheiro de sistema na fase de instalação.

II. MODELAÇÃO DA RESPOSTA IMPULSIVA

A resposta impulsiva do canal de propagação[3] pode ser escrita destacando o raio de linha de vista e os restantes raios por ordem de reflexão:

\[ h(t) = a_{\text{ref}} e^{-d_{\text{ref}} / t} \delta(t - t_{\text{ref}}) + \sum_{m=1}^{M} a_{m} \sum_{n=0}^{N_{m}} e^{-d_{m,n} / t} \delta(t - t_{m,n}) \]

\( a_{\text{ref}} \) representa a amplitude, normalizada em relação ao impulso transmitido, do primeiro raio que chega ao receptor após m reflexões. O tempo de atraso \( t_{m,n} \) é dado por \( t_{m,n} \), onde \( t_{m,n} \) é o comprimento do raio e \( c \) representa a velocidade da luz em espaço livre. O atraso de fase \( \phi_{m,n} \) engloba o desvio de fase devido às reflexões e à propagação em espaço livre. Analogamente, \( \phi_{\text{ref}} \) e \( \phi_{m,n} \) representam a amplitude, atraso e desfasamento do raio directo, e finalmente, \( M \) é a máxima ordem de reflexão considerada.

A PRN, definida como o quociente entre a potência recebida e potência transmitida, pode ser escrita na sua forma discreta como:

\[ PRN = \frac{P_{R}}{P_{T}} = a_{\text{ref}}^{2} + \sum_{m=1}^{M} \sum_{n=0}^{N_{m}} a_{m,n}^{2} \]

e o esforçamento do atraco (EA) definido em [3], pode ser obtido da seguinte forma:

\[ EA = \sqrt{t^{2} - c^{2}} \]

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